Advancing Wireless Sensor Networks Performance over Radio Trigger Wake-up Capabilities

Fatma Almajadub, Khaled Elleithy and Azza Shaer

Department of Computer Science and Engineering
University of Bridgeport
Bridgeport, CT, USA
falmajad@my.bridgeport.edu , elleithy@bridgeport.edu, aalshaer@my.bridgeport.edu

Abstract

In this Paper, we enhance the performance of Wireless Sensor Networks (WSNs) by optimizing the Wake-up capabilities within a passive radio-triggered wake-up circuit and then used its applications to manage the power consumption of the WSNs. The architecture of our proposed circuit manages the radio power consumption of WSN by harvesting energy from the radio signals and making the radio-triggered hardware sends a wake-up signal to the microcontroller (MCU) of the node. This harvest process takes only 15μs or less to produce wake-up signals within the wake-up circuit and prolongs the lifetime of the WSN nodes. In addition, the proposed circuit receives the RF signal of the network controller through the antenna node and produces an output voltage (VOL_{DC}) by its rectifier module so that this voltage produces direct current DC of 250 mV with the received power of 0.85uW (-13.85dBm). Most importantly, the proposed circuit can produce an output triggered voltage (VOL_{TG}) by its module of LTC1540 –Nano-power Comparator which works as an amplifier (VOL_{DC}) and only needs 0.3μA of energy for the setting of the threshold detector value within the long distance of 100m or more and radiation source of 2W in free-space. The simulation results demonstrate that the proposed circuit can produce VOL_{DC} and VOL_{TG} to trigger the wake-up signal of MCU within the long distance and low duty cycle as well as this circuit can identify the synchronization on WSNs.

Keywords: *(*WSNs) Wireless Sensor Networks, Passive Radio Trigger, Wake-up Circuit Capabilities, Low Power consumption.

1. Introduction

Since the radio transmission consumes most of the power in WSNs, good management of the radio triggered capabilities in WSN is the best way to optimize its performance.[1] However, the main challenge is to optimize passive radio triggered wake-ups capabilities; especially by optimizing the wake-up mode or sleep mode in order to reduce power consumption and cost of WSNs. Due to the increasing need of radio trigger capabilities on WSNs and its support by recent techniques, the sensor data can be derived anywhere on WSNs through several simple and cheap ways. These are provided by each node on WSN during sensing, storage, processing and communication capacities.

Many studies and researches of WSNs have shown that it is difficult to replace the batteries of sensor nodes. Thus, effective management of power consumption in WSNs is necessary for prolonging the lifetime of WSNs. Therefore, good power consumption management schemes can be implemented by exploiting wake-up and sleep schedule techniques in order to reduce the power consumption of nodes. Moreover, it is important to synchronize the received messages of the sensor nodes so that they are received only when the sensor nodes are in Wake-up mode.

There are many schemes to manage the power consumption of WSNs over radio trigger capabilities. Among those techniques that show good performance and serve our proposed work are the following techniques:

1) Wake-up and sleep schedule scheme [2].
2) A Stand-Alone Radio Receiver Wake-up scheme [3][4].
3) A Passive Radio-Triggered Wake-up Circuit Scheme.

2. The Concept of Passive Radio-Triggered Wake-up Circuit

This circuit consists of a set of diodes, capacitors, and inductors. The circuit is designed for the realization of the functions of the wake-up/sleep schedules so that this circuit has the ability to convert the input power of radio frequency signal (RF) to the voltage of direct current (DC). In addition, this circuit is based on the idea of the stand-alone radio receiver wake-up scheme so that this circuit can activate and shut down the nodes depending on a wake-up signal in the environment of WSNs. Therefore, this circuit can eliminate some wake-up periods which waste energy [5] [6].

2.1. WSNs System within the Passive Radio-Triggered Wake-Up Circuit:

The WSN within the passive radio-triggered wake-up circuit must be prepared with nodes and controllers. Figure 1 shows the structure of the node prepared with the passive radio-triggered wake-up circuit within WSN.

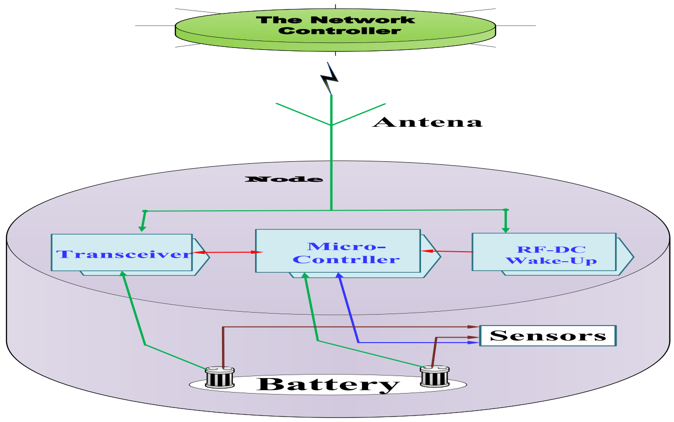

Figure 1: The Structure of Node Prepared with the Passive Radio-Triggered Wake-up Circuit within WSN

Figure 2 demonstrates that all nodes of WSN should be equipped with the same antenna which is linked with the transceiver device as well as with this circuit. In addition, RF-DC wake-up circuit sends a DC voltage directly to the microcontroller MCU of the node to stimulate and trigger the interrupted signal and wake-up the MCU instantly.

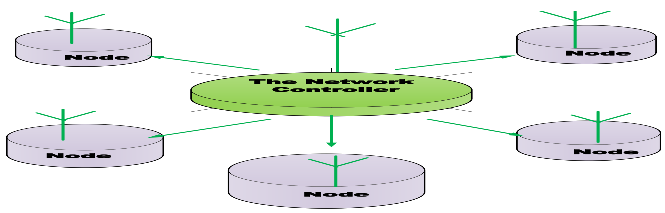

Figure 2: WNSs System within Passive Radio-Triggered Wake-up Circuit

One of advantages of this circuit is that it only needs low cost diodes, capacitors, and inductors. Another advantage, this circuit is a passive circuit, thus it does not need more energy. Therefore, it is the best choice for realizing power management in WSNs.

3. Proposed Model

In order to enhance the performance of WSNs over passive radio-triggered wake-up capabilities, we propose optimizing the circuit of passive radio-triggered wake-up. This circuit generally contains a set of modules which are the antenna, an impedance matching module, and a rectifier module. However, we try to improve these modules in order to achieve reasonable performance of the wake-up circuit. Thus it can be used by the WSNs node to achieve good power management in order to optimize radio trigger capabilities. The purpose of the proposed circuit is to receive RF signals in order to generate maximum input power of these RF signals and convert them to DC voltage (**VOL_{DC}**) in order to produce the desired output voltage. Thus, this circuit can amplify DC voltage to produce the output TG voltage (**VOL_{TG}**) in order to trigger the wake-up signals of MCU within long distance.

Our proposed circuit is designed to improve its components separately and to support the long distance from the network controller to the node antenna. Therefore, we propose to add another module to the general modules of this circuit which is LTC1540 – Nano-power Comparator in order to support the long distances between the network controller and the node antenna, as well as produce prefect output voltage at a maximum input power. This comparator may need extra power supply but it will not affect the whole circuit. However, without the LTC1540 – Nano-power Comparator module; the proposed circuit does not need power supply. To keep the node's power within the proposed circuit, we propose to provide external power supply to only the comparator without adding it to the entire circuit; thus, it will not share power with the circuit. Figure 3 shows the proposed circuit.

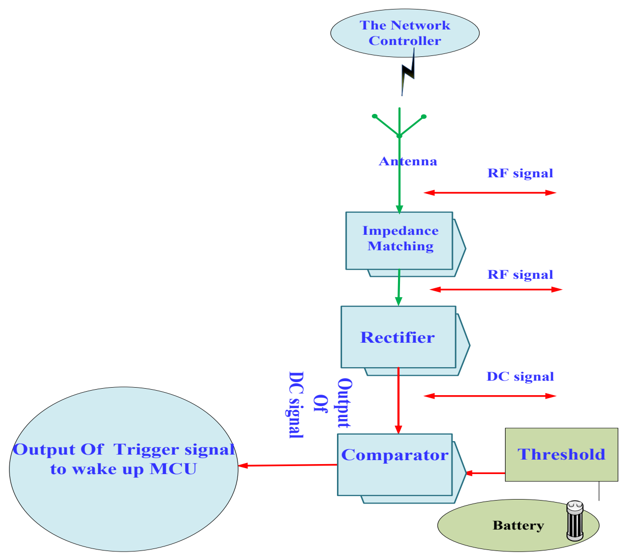

Figure 3: The Mechanism of the Proposed Passive Radio-Triggered Wake-up Circuit within its Modules

Each node of the proposed design of the wake up circuit's modules is equipped with:

1. Printed monopole antenna to function between circuit modules and its gain factor which is 0.40-0.63 joule.
2. Two impedance matching circuits by using the zero bias Schottky diode; which is called HSMS285C (series pair configuration) and is with SOT-323 package.

Furthermore, we propose the use of the multi-stages rectifier circuit so that each circuit contains some components like diodes, inductors, and capacitors which were used in [5] and [6]. However, in our design we add resistances for capacitors in order to join the high voltages within the proposed circuit and reduce the total impedance and resistance of the moving current into capacitors. Therefore, we used two diodes and four capacitors merged together with two resistances in one circuit. However, the multi-stage circuit module was proposed in many studies of radio-triggered wake-up circuits, but each study used a different design such as in [7], [8], [9] and [10]. These were costly designs for the passive RFID tags by adding the CMOS process. Although the design in [5] used a cheap design for the improvement of discrete components, [5] doesn't support the long distances between controller network and the node's antenna. Therefore, we targeted to design our proposed circuit module with the aim of improving long distances, flexibility, low cost, and prefect power management.

Furthermore, we propose to use the comparator module type LTC1540 – Nano-power with Reference to LT5400 Comparator [11]. The comparator module on our proposed circuit achieves the following functions:

1. The comparator can compare the DC voltage of 10mV or more with the threshold voltage.
2. The comparator can produce a high voltage trigger (VOL_{TG}) to wake-up the MCU of the node.
3. The comparator consumes less energy about 0.3uA;

3.1 The Proposed Impedance Matching Module

Two impedance matching circuits are used so that each circuit works as a linear equivalent circuit. We propose to use the zero bias schottky diode which is called HSMS285C (series pair configuration) and is with SOT-323 package shown in Figure 4. This diode helps representing the signals at small levels. Both circuits have the specifications given in Table 1. The impedance matching circuit is as shown below in Figure 5. The capacitors in the multistage rectifier are set to 0.30pF [5] [13].

Figure 4: HSMS-285C SCHOTTKY DIODE with SOT-323

Table 1: Specifications of The Linear Equivalent Circuit of the Schottky Diode" HSMS285C".

Parameters	Function	Value
Rjun (Rv)	The junction resistance of the diode	9 KΩ
Cjun1	The junction capacitance of the first diode	0.9 pF
Cjun2	The junction capacitance of the second diode	0.9 pF
Rc (RS)	The parasitic resistance is at the base of the chip and represents the losses in the bond wire and the bulk silicon of the diode	25 Ω
Lpc	The parasitic inductance and capacitance caused by the package	2nH
Cp1	The parasitic inductance and capacitance caused by the package	0.04pF
Cp2	The parasitic inductance and capacitance caused by the package	0.04pF

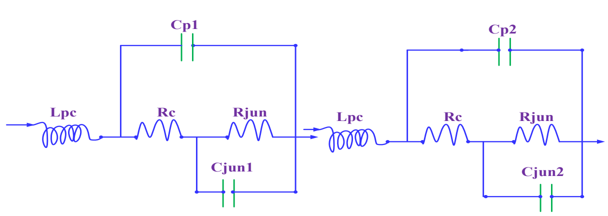

Figure 5: The Linear Equivalent Circuits Models of the HSMS285C Schottky Diode

3.2 The Proposed Multi-Stages Rectifier Module:

Each one-Stage rectifier module of our proposed circuit works to double the output voltage. The proposed one-Stage circuit contains the following components:

1) Two diodes DD1 and DD2 which are connected in series so that forward current can only travel from the ground potential to the positive terminal of the output voltage VOL_{out}. These diodes allow the forward current to move in one direction so that they work with other elements of the rectifier circuit to serve as a passage to the forward current when voltage is increased by a specific value. In addition, it helps to fix an alternating current (AC).

2) Four capacitors which work as follows:

i. The first one which called CP1 prevents the DC current from flowing and streaming into the circuit and helps the current to flow into CP2.

ii. The second one which called CP2 helps to keep the charge of the high frequency currents and allows the high frequency currents to flow into the circuit from DD1to DD2.

iii. The Third, known as the CP3, receives and keeps the resulting charge in the circuit.

iv. The fourth one which is called CP4 is for refining, revising and smoothening the output voltage VOL_{out}. Therefore, this circuit works as a pump so that CP1, CP2 and DD1 make up a DC-level like converter or shifter while CP3, CP4 and DD2 make up a peak-like detector device as is shown in Figure 4.

3) Two resistors (R1 and R2) are added to be used by the capacitors for uniting the voltage during the proposed circuit and for reducing the total impedance by merging resistances and capacitors together to reduce the voltage on capacitors to zero.

$$VOL_{cp1} = VOL_{cp2} = VOL_{cp3} = VOL_{cp4} = 0 \quad \text{.....(1)}$$

Thus, the current (Au) equals the voltage of circuit (VOL_{DC}) divided by the total resistance (R1+R2).

$$Au = VOL_{DC} / (R1+R2) \quad \text{.....(2)}$$

And capacitance (Cap) equals 1 divided by the total resistance (R1+R2).

$$Cap = 1 / (R1+R2) \quad \text{.....(3)}$$

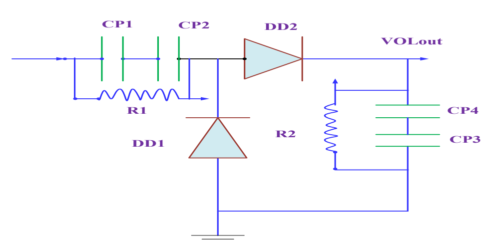

Figure 6: Show The One-Stage Rectifier circuit.

These kinds of rectifiers are necessary to design the proposed circuit. There is a certain amount of voltage that is necessary to trigger the microcontroller (MCU) of the node and the voltage of one stage circuit is not enough for it. Thus, when we change the voltage of the one-stage circuit from ground level to a DC voltage VOL_{DC}, the output voltage will be as follows:

$$VOL_{out}=4*(VOL_{Max} - VOL_{Dio}) + VOL_{DC}. \ \ldots.. (4)$$

Where VOL_{Max} is the maximum or peak voltage, VOL_{Dio} is voltage on diodes. Therefore, we can form and prepare the rectifier circuit with multistage by collecting and combining several One-Stage circuits so that the VOL_{DC} of each stage will work as the DC reference to next stage. Hence, VOL_{out} of M stages circuit is as follows:

$$VOL_{out} = 4*M*(VOL_{Max} - VOL_{Dio}) \ \ldots..(5)$$

3.3 The Proposed Comparator Module:

The comparator is an important module in our proposed circuit to support long distance, even though it needs extra energy (0.3uA) to set the threshold value which is not severe compared with other devices, such as the amplifier which needs 10A. Figure 7 shows the 2.9v Vcc threshold detector circuit of LTC1540 comparator with Nano-power. The parameters of the LTC1540 comparator with Nano-power 2.9v Vcc threshold detector are shown on Table 2.

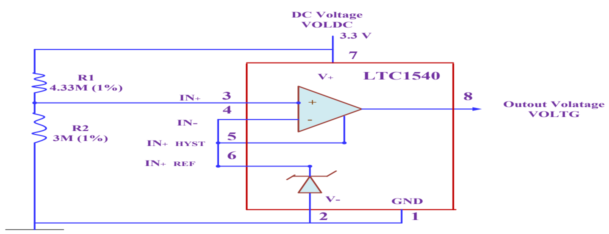

Figure 7: The 2.9v Vcc Threshold Detector.Circuit of LTC1540 Comparator with Nano-Power

Table (2): The Parameter of LTC1540 – Nano-power Comparator

Parameters	Function	Value
Cu	Ultralow Current	0.3µA
CI	Continuous Source Current	40mA
Z	Capacitor	0.01µF
Rws	Wide Supply Range	2V to 11V
OD	Overdrive	10mV
Dp	Propagation Delay	60µs
Vin	Input Voltage Range And Negative Supply Reference Output Sources	Up to 1mA
DFN	DFN Package	3mm x 3mm x 0.8mm

4. Implementation of the Proposed Wake-up Circuit

In this section, we discuss the implementation of the proposed rectifier circuit.

4.1 Counting the RF Input Power of the Proposed Module

The RF power (PW_{RF}) of RF signal received by the proposed wake-up circuit within passive radio-triggering by an impedance matching circuit is either from the one-stage circuit module or multi-stages circuit module. Thus, the parameters in Table 3 are used in equation (6).

Table (3): RF Signal Parameters

Parameters	Symbol
Sending Power or RF Signal Power	PW_s
Output1 of power at network controller's antenna	PO_cn
Output2 of power at node's antenna	PO_an
Wavelength of the electromagnetic wave	Λ
Distance between the network controller and the node.	D_rs

Therefore, the PW_{RF} is given by the equation (1)

$$PW_{RF} =[(PO\_cn * PO\_an * PW\_s *(\lambda^2)) / (4\pi* D\_rs)] \ \ldots..(6)$$

We found that we can increase the input power PWRF by increasing the distances D_rs. In the simulation, we used PW_s of 2W. The receiver power starts at 0.85uW (-13.85dBm) for 915MHz. Therefore, when PO_cn=2dB, λ=0.6.56,D_rs=100 or more, then PWRF or PW_s=3.4W (-55.4dBm).

As result, the input power or RF signal power (PW_{RF}) is at the maximum level when VOL_{Max} is very low. In addition, if the PW_{RF} is constant and not changed during the circuit, it will increase the VOL_{DC}, thus, VOL_{Dio} will be too low. Therefore, using the zero bias Schottky diode "HSMS285C" is the best choice for multi-Stage rectifier circuit.

4.2 Implementing the One-Stage Rectifier Module

The implementation of the proposed circuit is done by executing the mechanism of the circuit in Figure 3 and Figure 6. This circuit includes the RF signal that has two parts; the negative part and the positive part of the capacitors. As well as the voltages on these parts, which will be different; the voltage of positive part is double the voltage of negative part.

1) If the RF signal is negative and larger than the voltage into the DD1, the current will pass through DD1 and leads to move the charge from CP1 to CP2 while the DD2 is turned off. The voltage of the negative part on DD1 passes CP1and CP2 then to DD1 and moves from CP3 to CP4. The latter is VOL_{Dio1} which is the difference between the maximum negative part voltage VOL_{NMax} and the voltage on the DD1.

$$VOL_{Nout} = 2*(VOL_{NMax} - VOL_{Dio1}) \ldots..(7)$$

2) If the RF signal is positive and larger than the voltage into the DD2, the current will pass through DD2 and will transfer the charge from CP3 to CP4 while DD1 is turned off. Thus the voltage of positive part on DD2, which passes CP1and CP2 then to DD2 and to CP3 and CP4 ; is the difference between the maximum positive part voltage VOL_{PMax} and the voltage on the DD2 which called VOL_{Dio2}.

$$VOL_{Pout} = 4*(VOL_{PMax} - VOL_{Dio2}) \ldots..(8)(a)$$

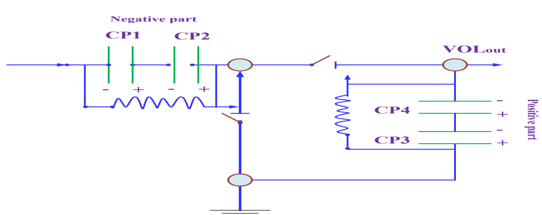

Figure 8: The One-Stage circuit within the negative part and the Positive Part of the capacitors

Therefore, the output voltage of one stage circuit (VOL_{DC}) is equal to the voltage passed in CP1 and CP2 (VOL_{in}). Adding to the 4 maximum positive input voltage (VOL_{Max}), and subtracting 4, the turn-on voltage on diode VOL_{Dio} is equal to:

$$VOL_{out=} VOL_{in+} 4*[VOL_{Max-} VOL_{Dio}] \ldots..(8)(b)$$

Where VOL_{in} is the voltage passed on CP1 and CP2 which according to (1) equal zero, thus;

$$VOL_{in=} VOL_{cp1} = VOL_{cp2} = 0.$$

Therefore, the output voltage of one-stage circuit is as following:

$$VOL_{DC=} 4*(VOL_{Max} - VOL_{Dio}) \ldots..(9)$$

4.3 Implementing the Multi-Stage Rectifier Module:

According to equation (9), when we have M stage circuit, the voltage would be given by (5).

$$VOL_{DC=} 4*M*(VOL_{Max-} VOL_{Dio}) \ldots..(10)$$

We can analyze and infer the following when we implement the Multi-Stage circuit:

1. We can add stages to our proposed circuit as it is required to convert RF signal to DC voltage until the last RF input voltage is transformed into the right value of VOL_{DC}.
2. We can add stages to our proposed circuit only until a certain level as we mention in the previous point. Adding more and more stages would lead to wasting the power and charge in the diodes and capacitors, thus the circuit with multi-stages will be less efficient. Therefore, we must determine the number of the stages that would give us the maximum DC voltage VOL_{out}. This number should be as far as the function of radio-triggered wake-up is needed.

4.4 Implementation of the Comparator Module

The implementation of the comparator circuit is done by executing the mechanism described in Figure 3 and Figure 7. This circuit includes focusing on the DC voltage (VOL_{DC}) which is produced from the rectifier module. The comparator module can amplify VOL_{DC} to TG voltage (VOL_{TG}) to be suitable with the long distance between the network controller and node's antenna. However, the VOL_{TG} is different based on these distances so that the VOL_{TG} is produced by following:

$$VOL_{TG} = VOL_{DC} + VOL_{HYST} + VOL_{REF.} \ldots.. (11)$$

However, we can choose the comparator to operate from a single supply (2V to 11V) or a dual supply (±1V to ±5.5V) so that it's hysteresis can be programmed by using two resistors R1 and R2 as well as the HYST pin. In addition, each input operates from the negative supply within 1.3V of the positive supply so that the output stage of comparator can reach to 40mA continuously.

As result, we infer that eliminating the power supply glitches is done by eliminating of the cross-conducting current that occurs normally when the comparator changes logic states. For long distances application, the LTC1540 is available in the 8-pin package, but for distance limited applications, the LTC1540 is available in a 3mm x 3mm x 0.8mm DFN Package

4.5 Implementing the Proposed Wake-up Circuit

We determine the following steps to implement the proposed wake-up circuit within passive radio triggering to achieve good management of the radio power consumption on WSN and harvest energy from the radio signals.

1. It provides a wake-up signal to the microcontroller (MCU) without using power supply from the harvest of radio-triggered hardware.
2. This harvest should only take 15µs in order to produce the wake-up signal within the circuit.
3. Receive the RF signal of network controller by antenna node.
4. The Wake-up circuit of a passive radio-triggering should produce an output voltage (VOL_{DC}) by its rectifier module so that this voltage is produced by a direct current DC of 250 mV with a received power as low as 0.85uW (-13.85dBm).
5. The Wake-up circuit of a passive radio-triggering must produce an output voltage (VOL_{TG}) by its module of LTC1540 –Nano-power Comparator which works as an amplifier to amplify (VOL_{DC}). It needs energy only of 0.3uA for the setting of the threshold detector value within the long distance of 100m or more and radiation source of 2W in free-space.

5. Simulation Results

In this section, we present the simulation results of the proposed wake-up circuit. These results include the optimization of its capabilities and modules. We choose Matlab software from Mathworks to simulate and implement the proposed impedance matching module, the multistage rectifier module and comparator module. The settings the simulation parameters are given in Table 4.

Table (4): Simulation Parameters

Parameter	Value
Distance between the network controller and the node (D_rs)	100 to 180 meters
Maximum simulation time	190 seconds
RF Signal Power	0.85uW
Output power at network controller's antenna	2dB
Wavelength of the electromagnetic wave	0.6.56
Output power at node's antenna	0.85uW (-13.85dBm).
Time for wake-up circuit	15 us
Power of Radio Frequency	3.4W (-55.4dBm).
DC voltage	250mV
PW of 2W	915MHz band
wake-up circuit at Input power PW_{RF}	7.85dBm, 9.85dBm, 11.85dBm and -13.85 dBm
comparator module	LTC1540
Antenna gain factors	0.63–0.40 joule
Energy of sensor	3.2 Joules
T_x energy	13 mW,
R_x energy	10 mW,
Stages of circuit	4
Resistance (R1-R2)	680 Ohm
The voltage of diode as SE diode VOL_{Dio}	0.7 v

We used the input power of the RF signal of 0.85uW (-13.85dBm) which is the result of equation (6). From Table (3), there are some elements that can produce a voltage higher than other elements of multistage circuit module because these elements have a higher quality factor. Therefore, we can produce high output voltage VOL_{DC} by using the multistage circuit with the elements which are higher VOL_{Max} and quality. We can also produce a higher voltage with a distance as long as 100m and transmitted power (PW_s) of 2W or more for 915MHz. Furthermore, the one stage circuit with good impedance matching circuit will produce a DC voltage of about 250mV by equation (9), but for multi-stages circuit module the voltage produced is given by equation (10). This harvest takes only 15µs for the wake-up circuit to produce the wake-up signal and prolong the lifetime of the WSNs nodes. For VOL_{TG} produced by equation (11) we can infer the following:

1. The resistances match the rectifier circuit module. Four capacitors should be used to uniform the capacitors' voltage and should be able to transform the flowing power and voltage of the antenna during impedance circuit module to the rectifier circuit module in order to achieve good impedance between the antenna and the rectifier circuit module. This impedance can increase the output voltage as well as reduce the loss of transmission.
2. The impedance matching circuit module can increase and amplify the output voltage. Although this increasing is passive, we can say that the theoretical efficiency of this increasing with maximum output voltage and power is achieved with the maximum quality factor.
3. Theoretically, we can argue that when the VOL_{Dio} is neglected, the VOL_{DC} could be double the whole voltage of the RF signal. On the simulation, we can't neglect the resistance of the capacitors CP1, CP2, CP3, and CP4 which makes the voltage of each capacitor equal to zero, thus; the value of the real output voltage VOL_{DC} should be less than its theoretical value. The proposed circuit should be able to exploit all the current as well as charge all the capacitors CP1, CP2, CP3, and CP4.

As a result, we improved the efficient modules of our proposed circuit to convert the input energy of RF signals to DC voltages and amplify it to TG voltage to be suitable for long distances. However, we used this circuit with multi-stage circuit module when the output voltage of the RF signals is very low in order to double the output voltage.

The Figure 9, Figure 10 and Figure 11 show the simulation results of the VOL_{DC} of multi-stages at different input power (PW_s).

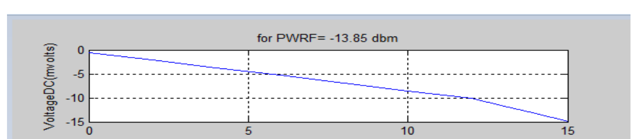

Figure 9: The Output Voltage VOL_{DC} of passive radio-triggered wake-up circuit at Input power PW_{RF} of -13.85 dBm

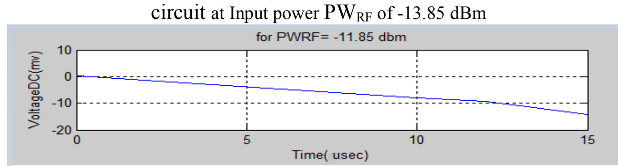

Figure 10: The Output Voltage VOL_{DC} of passive radio-triggered wake-up circuit at Input power PW_{RF} of -11.85 dBm

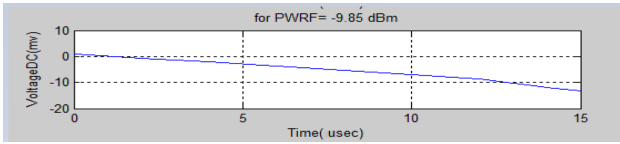

Figure 11: The Output Voltage VOL_{DC} of passive radio-triggered wake-up circuit at Input power PW_{RF} of -9.85dBm

The Figure 12, Figure 13 and Figure 14 show the simulation results of the VOL_{TG} of passive radio-triggered wake-up circuit at different distances D-rs.

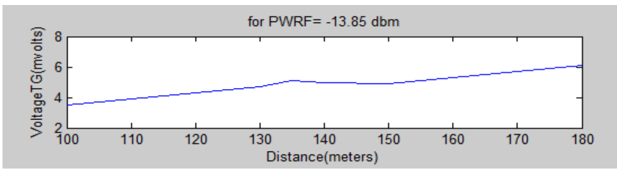

Figure 12: The Output Voltage VOL_{TG} of passive radio-triggered wake-up circuit at 130 M

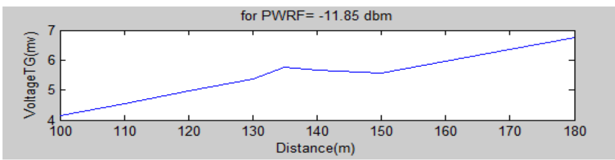

Figure 13: The Output Voltage VOL_{TG} of passive radio-triggered wake-up circuit at 124 M

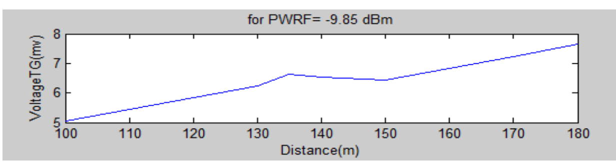

Figure 14: The Output Voltage VOL_{TG} of passive radio-triggered wake-up circuit at 120 M.

6. Conclusions

In this Paper, we have presented several techniques for enhancing the performance in WSNs over radio-triggered wake-up capabilities by optimizing the modules of the passive radio-triggered wake-up circuit as well as exploring its application in the power consumption management of WSNs. The simulation results demonstrate that we were able to manage the radio power consumption of WSN by harvesting energy from the RF signal and sending a wake-up signal to the node's MCU. We found that this harvest takes only 15µs or less to produce wake-up signals within the wake-up circuit and prolongs the lifetime of the WSN nodes.

The proposed circuit receives the RF signal of the network controller through the node antenna and produces VOL_{DC} by its rectifier module so that this voltage is 250 mV. This circuit can produce the VOL_{TG} by its comparator module which can compare the VOL_{DC} of 10mV or more with a threshold voltage and produce a high VOL_{TG} which is able to wake-up the MCU of the node. We found that the comparator can consume less energy; only 0.3uA which is enough to amplify VOL_{DC} for a long distance of 100m or more and radiation source of 2W in free-space. Furthermore, the proposed circuit achieves synchronization of WSNs within long distances as well as it consumes low power consumption within these long distances. Furthermore, the simulation results show that the proposed circuit can produce and amplify a higher voltage with a long distance so that it is enough to reduce the energy consumption from 13.85% to 21.85 %.

Finally, we can say that the vast majority of the system energy in a wireless sensor node is consumed by the radio. Accordingly, we reduced this consumption either by decreasing the transmission output power or by decreasing the radio duty cycle. For future work, we plan to improve the proposed circuit by using mechanisms that make the nodes addressable so that only the node which is addressed with the RF signal goes into the wake-up mode while all other nodes stay in sleep mode.

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